AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data processor ~~for demodulating a series of data including the~~ predetermined mark for detecting synchronization, comprising:

a receiving unit for receiving ~~the~~ a series of data including predetermined marks for detecting synchronization ~~in a plurality of parallel bits~~ and generating a plurality of parallel data from the series of data; and

a plurality of detecting ~~unit~~ units for detecting said predetermined ~~mark~~ marks for detecting synchronization from the plurality of parallel data.

2. (Currently Amended) A data processor according to claim 1, wherein said plurality of detecting ~~unit detects~~ units detect the predetermined marks ~~mark~~ for detecting synchronization in a predetermined bit width among the series of data in ~~the~~ parallel condition.

3. (Currently Amended) A data processor according to claim 1, further comprising a generation timing selecting unit for selecting ~~the~~ generation timing of the a window for detecting the predetermined marks ~~mark~~ based on the predetermined ~~mark~~ marks for detecting synchronization.

4. (Currently Amended) A data processor according to claim 1, further comprising a data demodulating unit for demodulating the series of data between the predetermined marks for detecting synchronization based on the predetermined ~~mark~~ marks for detecting synchronization.

5. (Currently Amended) A data processor according to claim 1, further comprising a detection line memory unit for storing ~~the~~ a detection line based on the predetermined ~~mark~~ marks for detecting synchronization.

6. (Currently Amended) A data processor according to claim 1, further comprising a data selecting unit for selecting ~~the~~ data based on the predetermined ~~mark~~ marks for detecting synchronization.

7. (Currently Amended) A data processor according to claim 1, further comprising a data counting unit for counting the series of data between the predetermined ~~mark~~ marks for detecting synchronization based on the predetermined marks for detecting synchronization.

8. (Canceled).

9. (Currently Amended) A data processor according to claim 1, wherein said receiving unit is provided with a shift register to input the ~~data of a plurality of parallel bits~~ plurality of parallel data connected with the detecting ~~unit~~ units in the same number as the number of parallel ~~bits~~ data.

10. (Currently Amended) A data processor for detecting ~~the~~ predetermined ~~mark~~ marks for detecting synchronization included in a series of data read from ~~the~~ a memory medium in order to establish ~~the~~ synchronization at the a time of transferring the series of data to the a

controller unit from the a read channel unit, ~~and for demodulating the series of data between the predetermined marks for detecting synchronization,~~ comprising:

a receiving unit for receiving the series of data including predetermined marks for detecting synchronization ~~in a plurality of~~ parallel bits and generating a plurality of parallel data from the series of data; and

a plurality of detecting unit units for detecting said predetermined ~~mark~~ marks for detecting synchronization from the plurality of parallel data.

11. (Currently Amended) A data processing method ~~for demodulating a series of data including the predetermined mark for detecting synchronization,~~ comprising the following steps of:

receiving ~~the~~ a series of data including predetermined marks for detecting synchronization ~~in a plurality of parallel bits~~;

generating a plurality of parallel data from the series of data;

detecting the predetermined ~~mark~~ marks for detecting synchronization from the said plurality of parallel data to establish ~~the~~ synchronization of the series of data; and

demodulating the series of data based on the predetermined ~~mark~~ marks for detecting synchronization included in the series of data.

12. (Currently Amended) A data processing method according to claim 11, wherein the predetermined ~~mark~~ marks for detecting synchronization are detected in a predetermined bit ~~width~~ widths of the series of data in ~~the~~ parallel condition.

13. (Currently Amended) A data processing method according to claim 11, wherein ~~the~~ generation timing of the a window for detecting predetermined ~~mark~~ marks is selected based on said the detected predetermined ~~mark~~ marks for detecting synchronization.

14. (Currently Amended) A data processing method according to claim 11, wherein ~~the~~ a detection line is stored based on the detected predetermined ~~mark~~ marks for detecting synchronization.

15. (Currently Amended) A data processing method according to claim 11, wherein data is selected based on the detected predetermined mark marks for detecting synchronization.

16. (Original) A data processing method according to claim 11, wherein data between the detected predetermined marks for detecting synchronization is counted up.

17. (New) A data processor according to claim 1, wherein said plurality of detecting units detect the corresponding each of the plurality of parallel data.